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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LUHRS, MICHAEL K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,918	USUI ET AL.	
	Examiner	Art Unit	
	Michael K. Luhrs	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *updated search history*.

DETAILED ACTION

Drawings

1. The replacement drawings were received on 07 October 2004. These drawings are approved.

Claim Objections

2. Claim 8 is objected to because of the following informalities: the claim reads "after performing the plasma irradiation using oxygen gas..." however claim 1 does not stipulate irradiation using *oxygen gas,* and therefore the step of "after" cannot occur. Please stipulate a positive recitation of the irradiation using *oxygen gas*, as a step which sets forth the irradiation using oxygen gas (in either claim 1 or 8). Then, the further step, i.e. the "after" step, of plasma irradiation using the inert gas, can be presented. Appropriate correction is required.

3. Claim 2 is objected to because of the following informalities: in lines 2-3, "...locations that are to become pad" suggest changing "pad" to read –pads-- (i.e. plural since "locations" is plural). Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 1-4, 6-7, and 9-10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et. al. USPN 6,689,641 in view of Haji et. al. USPN 5,909,633.

Regarding claim 1, *forming conductive films that are laminated in multiple layers with interlayer insulating layers interposed in between*; Ohta et. al. teach laminated layers, line 12, column 10, first resin layer '7', line 24, column 10, second resin layer '9', lines 30-1, column 10; conductive layer 27, line 40, column 10, second conductive layer,'29', line 45-6, column 10 all in Fig. 1; *forming a conductive wiring layer by selective removal of*

the conductive film at a top surface; Ohta et. al. teach top surface of conductive layer '31' is predetermined patterned, line 51, column 10; *forming through holes in the interlayer insulating layers and forming connection means in the through holes to electrically connect the conductive wiring layer with the conductive film at a rear surface*; Ohta et. al. teach through holes '14', lines 17-8, column 10, rear surface line 7, column 10.

Ohta et. al. are silent regarding *affixing and electrically connecting circuit element to the conductive wiring layer*; and Ohta et. al. are silent on *irradiating plasma onto the conductive wiring layer, including the circuit element; and forming a resin layer so as to cover the circuit element.* Notice that, Haji et. al's substrate '11' and internal wiring '18' could inherently include all the processes that Ohta et. al. teach for their substrate.

Regarding the limitations that Ohta et. al. lack: Haji et. al. teaches the *affixing and electrically connecting circuit element to the conductive wiring layer; irradiating plasma onto the conductive wiring layer, including the circuit element; and forming a resin layer so as to cover the circuit element.* The particular citations in the Haji et. al. reference are: the chip element '12' is affixed from Figure 2 to Figure 3, (lines 50-52, column 2); by bonding to substrate '11' (lines 10-11, column 3), irradiating plasma in Figure 5, (lines 12-30, column 4), including the chip element '12', which is present in Figure 5 during irradiation, and resin layer '19' is formed in Figure 7, (lines 34-36, column 4), electrical connection is made by the gold wire '15' to electrode '14' to *electrically connect(ing)* [the] *circuit element* ['12'] *to the conductive wiring layer*, i.e. gold layer '23', viz, and further to the internal wiring layer '18'.

Since Haji et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Haji et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to *affixing and electrically connecting* chip order to connect the chip to a substrate and irradiating for the purpose of preparing the wiring pads for the bonding attachment with motivation of enhanced bonding of the metal wiring to the conductive layer of the substrate (Haji et. al. lines 62-67, column 6).

Regarding claim 2, Ohta et. al. teach resin layer '11', line 15, column 10, wherein the conductive wiring layer is covered with resin while exposing locations that are to become pads, e.g. pads '32' of conductive layer '31', lines 53-56, column 10.

Regarding claim 3, Ohta et. al. lack *wherein in the step of irradiating plasma, the plasma is irradiated onto a top surface of the resin as well to roughen the top surface of the resin while a voltage, which is charged up in the resin, is released from the conductive wiring layer and via the conductive films.* Haji et. al. provide electrode 44 which makes the connection via the conductive layer of substrate 11 as shown in Fig. 5, plasma irradiation occurs both on the pads and substrate, (see lines 26-29, column 4) for the purpose of roughening for enhanced bonding. The top surface of the substrate is molded with resin (lines 20-21, column 3). Since Haji et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Haji et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to utilize the plasma irradiation to enhance the bonding.

Regarding claim 4, Ohta et. al. teach wherein connection means, comprising a plating film, are formed in the through holes to electrically connect the conductive wiring layer and the conductive film, as seen in Fig. 1 showing through holes: '14', (lines 17-8, column 10), e.g. plating '15', lines 20-1, column 10, comprised of plating (lines 4-6, column 13), connecting to '27' , (line 40, column 10), is a conductive film, (lines 11-12, column 13).

Regarding claim 6, Ohta et. al. is silent on the inert gas, such as Argon, Neon, or Helium. Haji et. al. teach *Argon* in line 17, column 4 for argon ions to impinge the substrate to provide a roughened area for bonding. Since Haji et. al. and Ohta et. al. are all from the same field of endeavor, the purpose disclosed by Haji et. al. would have been recognized in the pertinent art of Ohta et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to utilize the *argon* inert gas to prepare the metal for bonding without introducing other elements which could react with the metal and affect the bonding undesirably.

Regarding claim 7, Ohta et. al. silent on energy range. Haji et. al. teach energy as high frequency voltage (lines 19, column 4), is presumed within a range of 40eV to 100eV, since this is the result effective variable to optimize for the best bond. One having ordinary skill in the art would have looked to this variable in order to optimize the affect of the etching of the pad in order to produce the best results for the bonding thereafter. See optimization, MPEP 2144.05 [R-1] II, A, and *in re Aller.*

Regarding claim 9, Ohta et. al. teach that *the conductive film is formed of a metal having copper as a principal material* as described in line 65, column 12.

Regarding claim 10, Ohta et. al. are silent of *wherein the circuit element is semiconductor element that is electrically connected via metal wires to the conductive wiring layer. The circuit element is semiconductor element* is taught by Haji et. al.. as chip '12', *is electrically connected via metal wires to the conductive wiring layer* of substrate '23' by wiring '15'. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to connect a chip as shown by Haji et. al. Fig. 6 to a substrate '11' having conductive wiring layer taught by Ohta et. al., because the examiner has already pointed out that Haji's et. al. substrate could inherently posses all the features presented by Ohta's et. al. substrate and certainly one having ordinary skill in the art would have looked to the manner of producing the substrate as taught by Ohta et. al. and made the connection thereto using the method taught by Haji et. al. because such is well known for providing the connection of the chip to the substrate, viz, wire bonding of a chip to a substrate is well known for making a computer system.

Regarding claim 13, Ohta et. al. lack the selective removal of rear wiring after plasma irradiation, however Haji et. al. teach the irradiating (Fig. 5, discussed above) and then Haji et. al. actually flips the chip and substrate to expose the rear pads and again selectively irradiates (in Figure 14) the rear pads, selectively removing, etching the gold on the rear pads similarly to the above. It would have been obvious to one having ordinary skill in the art to do so, for substrate connection, to another substrate, or a second chip be connected to the substrate's opposite side. It would have been obvious to one having ordinary skill in the art to prepare the pads on the opposite side selectively removing the electrode outer layer in order to prepare these pads as well, for a good bonding connection.

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et. al. and Haji et. al. as applied to claim 1 above, and further in view of Yew et. al. USPN 6,602,803.

Regarding claim 11, Ohta et. al. and Haji et. al. are silent on a mounted chip in face down manner. Yew, et. al. show chip '10' having surface '10a' face is down against substrate '11' as shown in Fig. 1 for supplying the chip to a substrate of an IC package. Since Yew et. al. and Ohta et. al. and Haji et. al. are all from the same field of endeavor, the purpose disclosed by Yew et. al. would have been recognized in the pertinent art of Ohta et. al. and Haji et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art that a chip could also be provided in a face down manner as an alternative to build the IC, and to permit the active area of the chip to be connected to the substrate of an IC package as shown by Yew et. al.'s Fig. 1.

Regarding claim 12, wherein the circuit element is electrically connected to the conductive wiring layer via soft solder or other solder material: the conductive layer '31' in Ohta in lines 54-56, column 10, is prepared explicitly to mount electronic parts such as the IC chip (line 56, column 10) although silent on the solder. Haji et. al.'s substrate having the pad is electrically connected to the wiring by using wiring bonding (line 34, column 4). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to connect the conductive wiring of the substrate to the circuit element i.e. such as a chip, and that wire bonding is a method which uses solder to make the connecting bond.

8. Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et. al. and Haji et. al. as applied to claim 1 above, and further in view of Fu et. al. USPN 5,807,787.

Ohta et. al. and Haji et. al. lacks the use of oxygen plasma onto the conductive wiring. Fu et. al. teach that it is well known that oxygen plasma has been used to open the area over the bonding pad and in order to rid the surface of any residual polyimide so that the complete pad surface is available for wire bonding. Since Fu et. al. and Ohta et. al. and Haji et. al. are all from the same field of endeavor, the purpose disclosed by Fu et. al. would have been recognized in the pertinent art of Ohta et. al. and Haji et. al.. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to irradiate an oxygen plasma for the purpose of removing polyimide to expose the pad as taught by Fu et. al. before subjecting the exposed pad to an argon plasma treatment as taught by Haji et. al. in order to prepare the pad for wire bonding since this is a conventional procedure.

Response to Arguments

9. Applicant argues that the Yew et. al. reference uses the plasma irradiating for the purpose of bonding the chip to the substrate with the polyimide. Applicant also argues that in the Yew et. al. reference the only exposed metallization is the bonding pads, the examiner points out that the applicant's conductive layer 'exposed locations' are the bonding pads as expressed in applicant's claim 2. Apparently the applicant is merely pointing out that the conductive wiring layer be inclusive of the conductive film laminate, albeit this is already included in applicant's claim. Yew et. al. have an exposed conductive layer on the substrate (i.e. the bonding pads on the substrate). In regards to applicant's argument that the irradiation of plasma is *prior to* the chip attachment in Yew: At present, the applicant's claim wording of *affixing and electrically connecting the circuit element*, can occur, before or after, the *irradiating of plasma*, in claim 1, (notice the term "comprising" requires that either sequences be considered, viz, et.

al.), the examiner points out that the applicant can certainly amend the claim with language that would designate a specific sequence. The examiner withdraws the Yew reference because of the difference to *purpose*. The new reference to Haji et. al. teaches that the chip (12) and conductive wiring layer (within substrate 11 and as pads 14) are all present during irradiation in Fig. 5 and the purpose is consistent with the applicant's invention: It turns out that the Haji et. al. reference also teaches subject matter that was deemed allowable in previous action, therefore examiner withdraws the allowable matter of the previous action. The examiner discussed the new reference with the applicant's attorney, however the new rejection was requested be provided in written form.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Sugihara USPN 6,713,376 and 6,406,991 plasma treat interior of bump holes. Frautschi USPGPUB 2004/0234703 teach oxygen plasma clean and argon sputter clean. Jang USPN 6,096,649 teaches top metal and passivation procedure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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12/30/04

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